Small Signal Amplifiers - BJT

Definitions
Small Signal Amplifiers
Dimensioning of capacitors
Small signal condition
When the input signal ($v_{in}$ and, $i_{in}$) is small so that output signal ($v_{out}$ and, $i_{out}$) is confined in the active region of the output characteristics of the device, the device is operating in a condition of small signal. More specifically, the condition of small signal are verified when the variations in output are so small that the parameter values of the device can be regarded as constant.
In these conditions, the amplifiers can be analyzed using the small-signal models of the BJT. The small signal conditions occur, in general, for the first stages constituting an amplification system.

Linearity
In conditions of the small signal, the amplifier can be considered linear. The output signal is proportional to the input signal. This property derives from the fact that the components of the circuit are described by linear equations. If the system is linear applies the principle of superposition.

Amplitude and phase distortion
So that a waveform is not altered across the amplifier is necessary that each of its sinusoidal component is equally modified in amplitude and phase.
Definitions (2)

**Transfer function or network function**

Complex function that describes the *relationship* between the *output* signal and the *input* signal. It is defined in the Laplace domain (s) or in the frequency domain (s = jw).

**Amplitude and phase response**

Real functions obtained by specifying *amplitude* and *phase* of the transfer function with s = jw. Describe the variation of modulus and phase when the frequency changes.

**Gain and phase shift of an amplifier**

In the case of an *amplifier* transfer function is also called *amplification (or gain)* and can be expressed in *magnitude* and *phase*. Relatively to the various electrical quantities considered for entry and exit there are various definitions of gain.
**Definitions (3)**

**Input impedance**
It is the impedance viewed by the source of the input signal.

\[ Z_{in} = \frac{V_{in}}{I_{in}}; \]

**Output Impedance**
It is the impedance viewed from the output port. This impedance can be interpreted as the Thevenin impedance at the output port.

\[ Z_{out} = \frac{V_{out}}{I_{out}}; \]
Definitions (4)

Three configurations can be considered

**Common Base Conf.**

**Common Emitter Conf.**

**Common Collector Conf.**

<table>
<thead>
<tr>
<th>$R_P = R_1 \parallel R_2$</th>
<th>CBC</th>
<th>CEC</th>
<th>CCC</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A_v$</td>
<td>$\frac{h_{fe} R_C \parallel R_L}{h_{ie}}$</td>
<td>$- \frac{h_{fe} \cdot (R_C \parallel R_L)}{h_{ie} + (1 + h_{fe}) R_E} \approx \frac{R_C \parallel R_L}{R_E}$</td>
<td>$\frac{(1 + h_{fe}) \cdot R_E \parallel R_L}{h_{ie} + (1 + h_{fe}) \cdot R_E \parallel R_L} \approx 1$</td>
</tr>
<tr>
<td>$A_i$</td>
<td>$A_v \frac{R_{in}}{R_L} \approx \frac{R_C}{R_C + R_L} \frac{h_{fe}}{1 + h_{fe}}$</td>
<td>$A_v \frac{R_{in}}{R_L}$</td>
<td>$A_v \frac{R_{in}}{R_L} \approx \frac{R_{in}}{R_L}$</td>
</tr>
<tr>
<td>$R_{in}$</td>
<td>$R_E \parallel \frac{h_{ie}}{1 + h_{fe}}$</td>
<td>$R_P \parallel \left( h_{ie} + (1 + h_{fe}) R_E \right) \approx R_P$</td>
<td>$R_P \parallel \left( h_{ie} + (1 + h_{fe}) \cdot R_E \parallel R_L \right) \approx R_P$</td>
</tr>
<tr>
<td>$R_{out}$</td>
<td>$R_C$</td>
<td>$R_C$</td>
<td>$R_E \parallel \frac{(h_{ie} + R_P \parallel R_S) \cdot R_L}{(1 + h_{fe})}$</td>
</tr>
</tbody>
</table>

Electronics: a systems approach by N. Storey
Definitions (5)

Common Base C.

Common Emitter C.

Common Collector C.
Common Emitter C.

The voltage supply \((V_{CC})\) for the signal is equivalent to a short circuit.

Capacitors in the mid-band are equivalent to a short circuit.

\[
R_{in} = R_1 // R_2 // \left(h_{ie} + (1 + h_{fe}) R_E \right) \approx R_1 // R_2 = R_p
\]

\[
v_{out} = -i_b h_{fe} \cdot \left(R_C // R_L \right) \quad v_{in} = i_b \left(h_{ie} + (1 + h_{fe}) R_E \right)
\]

\[
A_v = \frac{v_{out}}{v_{in}} = \frac{h_{fe} \cdot \left(R_C // R_L \right)}{h_{ie} + (1 + h_{fe}) R_E} \approx \frac{R_C // R_L}{R_E}
\]

\[
A_i = \frac{i_L}{i_{in}} = \frac{v_{out}}{R_C // R_L} \frac{1}{v_{in} R_{in}} = A_v \frac{R_{in}}{R_C // R_L}
\]
Common Collettor C.

The voltage supply \((V_{CC})\) for the signal is equivalent to a short circuit.

\[ R_{in} = R_1 \parallel R_2 \parallel (h_{ie} + (1 + h_{fe})R_E \parallel R_L) \approx R_1 \parallel R_2 = R_P \]

\[ v_{out} = -i_b (1 + h_{fe}) \cdot R_C \parallel R_L \quad v_{in} = i_b (h_{ie} + (1 + h_{fe})R_C \parallel R_L) \]

\[ A_v = \frac{v_{out}}{v_{in}} = \frac{(1 + h_{fe}) \cdot R_E \parallel R_L}{h_{ie} + (1 + h_{fe}) \cdot R_E \parallel R_L} \approx 1 \]

\[ A_i = \frac{i_L}{i_{in}} = \frac{v_{out}}{R_C \parallel R_L} \frac{1}{v_{in}} = A_v \frac{R_{in}}{R_C \parallel R_L} \approx \frac{R_{in}}{R_C \parallel R_L} \]

Capacitors in the mid-band are equivalent to a short circuit.
Definitions (6)

**Coupling capacitor**
The amplifier is used to provide voltage and current levels adequate to drive the load connected to the output. The use of a single BJT is sometimes not sufficient to achieve this result. This limitation can be overcome by connecting in cascade several amplifiers, so that the signal emitted by the source is increased by each amplifier constituting the cascade. Each individual amplifier is called stage.

- Capacitors are used to connect one stage to another, they are referred coupling capacitors.
- The coupling capacitors have the function of providing insulation in DC so that the bias of one stage does not affect that of the next stage.
- These capacitors have to pass the AC signal from one stage to another with minimum distortion.
Definitions (7)

**By-pass capacitors**
These capacitors are connected in parallel to a resistor, so AC signals on the resistor are short circuited. In this way the AC and DC circuits are different.

For example, in the case of CEC, a by-pass capacitor on $R_E$ allows to obtain a higher voltage gain.

For the capacitor by-pass the following configurations can be used:

\[
A_v = \frac{h_{fe} \cdot (R_C // R_L)}{h_ie + (1 + h_{fe}) R_E}
\]

Gain variation with frequency
Because of the introduced reactive elements and the parasitic reactive elements the response of the amplifier is function of frequency.
Mid-band

- To simplify the study, it is useful to assume that there is a range of frequencies (bandwidth) in which all the reactive effects are negligible.
- Therefore in this range, gain ($A_0$), input and output impedances are real quantities ($R_{in}$, $R_{out}$).
- Three different frequency ranges (low, medium and high frequencies) can be considered.
- Three different frequency ranges correspond to three different dynamic circuits.

Cut-off frequencies

The mid-band is delimited by two frequencies, the lower cut-off frequency $f_l$ (determined by coupling and by-pass capacitors) and the upper cut-off frequency $f_u$ (determined by the junction capacitance and the parasitic effects).

The cutoff frequencies are defined by:

$$ |A(f_l)| = |A(f_u)| = \frac{A_0}{\sqrt{2}} $$

$$ |A(f_l)|_{dB} = |A(f_u)|_{dB} = |A_0|_{dB} - 3dB $$

Definitions (8)

Electronics: a systems approach by N. Storey (13.7)
Definitio

\[
A_v = \frac{V_L}{V_{in}} = \frac{|V_L|}{|V_{in}|} e^{j(\varphi_L - \varphi_{in})} = \frac{|V_L|}{|V_{in}|} e^{j\varphi_L};
\]

\[\varphi_{in} = 0\]

Common Emitter C.

Common Collector C.

Mid-band
Observation

• When the small signal conditions are verified the bias conditions are not influenced by signals present, and the full analysis can be divided into two sub-analysis: DC and AC.
• The AC analysis is often made by assuming the existence of the intermediate band and analyzing the circuit in this band, where the reactive effects can be neglected.
• Therefore, it is important to know the cutoff frequencies that define the mid-band.

Synthesis of a small signal stage

In general, a synthesis process, without the computer aid is carried out taking into account the behavior of the circuit in DC and in AC and estimating the effect of the capacitors on the cut-off frequencies. At last, the synthesis, of a stage which works at small signal, can be realized in the following steps:

1. Synthesis of the bias network.
2. Change of the bias network to meet the design specifications.
3. Choice of the capacitors to obtain the request lower cutoff frequency.
Small signal amplifiers
To design an amplifier, that by means of a suitable $R_L$ value, ensure a **specific current gain** and **voltage amplification equal to one**.

$$A_I = \frac{I_L}{I_{in}}$$

The circuit solution is the:

**common collector stage**

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**Synthesis steps**

1. Synthesize the bias network ($R_1$, $R_2$, $R_E$).
2. Select the $R_L$ value which ensures the desired current gain.
3. Choose the appropriate values for $C_1$ and $C_2$ which ensure the lower cutoff frequency given in the project specifications.
Synthesis steps: 1

Synthesis of bias network for the CCC

Bias network for the CCC

{3 resistors
3 relations

1) \( V_{CC} = V_{CE} + R_E \cdot (I_{CQ} + I_{BQ}) \)

2) \( I_2 \gg I_{BQ} = \frac{I_{CQ}}{h_{FE}} \)

\[ R_2 \leq \frac{R_{base}}{10} = \frac{1}{10} \left( \frac{V_{BEQ}}{I_{BQ}} + \frac{V_E}{I_{BQ}} \right) = \frac{1}{10} \left( \frac{V_{BEQ}}{I_{BQ}} + (1 + h_{FE}) \cdot R_E \right) \Rightarrow R_2 \leq \frac{1}{10} \cdot h_{FE} \cdot R_E \]

3) \( \frac{V_{CC} \cdot R_2}{R_1 + R_2} = R_1 \parallel R_2 \cdot I_{BQ} + (V_{BEQ} + V_E) \approx (V_{BEQ} + V_E) \)

\[ R_1 = \frac{V_{CC} - (V_{BEQ} + V_E)}{V_{BEQ} + V_E} \cdot R_2 \]
Synthesis steps: 1

Synthesis steps of bias network:

1) Choose the supply voltage $V_{CC}$ and the transistor working point: $I_C$, $V_{CE}$.

2) From the datasheet $V_{BEon}$ and $h_{FE}$ values can be obtained.

$$V_{BEon} = 0.66 \text{ V}$$
$$h_{FE} = 210$$

3) $R_E$ is obtained by:

$$R_E = \frac{V_{CC} - V_{CEQ}}{I_C} = \frac{20 \text{ V} - 10 \text{ V}}{10 \text{ mA}} = 1 \text{ k}\Omega$$

4) $R_2$ is obtained by:

$$R_2 \leq \frac{1}{10} \cdot h_{FE} \cdot R_E = \frac{210 \cdot 1 \text{ k}\Omega}{10} = 21 \text{ k}\Omega \Rightarrow R_2 = 15 \text{ k}\Omega$$

Or:

$$R_2 = \frac{V_{BE} + V_{E}}{I_2} \leq \frac{V_{BE} + V_{E}}{10I_C} h_{FE}$$

5) $R_1$ is obtained by:

$$R_1 = \frac{V_{CC} -(V_{BEQ} + V_{E})}{V_{BEQ} + V_{E}} \cdot R_2 = \frac{9.34}{10.66} \cdot 15 \text{ k}\Omega \approx 13 \text{ k}\Omega \Rightarrow R_1 = 12 \text{ k}\Omega$$
Synthesis steps: 2

\( R_L \) is obtained by the circuit analysis.

\[
R_p = R_1 \parallel R_2 = \frac{R_1 \cdot R_2}{R_1 + R_2}
\]

\[
A_I = A_v \cdot \frac{R_{in}}{R_L} \approx \frac{R_p \parallel \left( hie + (1 + h_{fe}) \cdot R_E \parallel R_L \right)}{R_L} \quad \rightarrow \quad \frac{1}{R_L A_I} \approx \frac{1}{R_p} + \frac{1}{h_{fe} R_E \parallel R_L}
\]

\[
h_{fe} \left( \frac{1}{R_L A_I} - \frac{1}{R_p} \right) \approx \frac{R_E + R_L}{R_E \cdot R_L}
\]

\[
R_E \left( \frac{h_{fe}}{A_I} - 1 \right)
\]

\[
R_L \approx \frac{1 + \frac{h_{fe} R_E}{R_p}}{A_I}
\]

If \( h_{fe} R_E \gg R_p \) or \( h_{fe} R_E > 10R_p \)

If \( h_{fe} R_E > 10R_p \) and \( h_{fe} > 10A_I \)

\[
R_L \approx \frac{R_p}{A_I}
\]

\[
R_L \approx \frac{6.666k\Omega}{10} \approx \frac{6.8k\Omega}{10} = 680\Omega
\]
To perform the $A_I$ and $R_{in}$ measurements:

Mount the circuit introducing a test resistor $R_T$  

$R_T = R_1 // R_2 = 6.8k \Omega$

Measure $V_{RT}$ (using two probes)

Calculate $I_{in}$ and $I_L$

$I_{in} = \frac{V_{RT}}{R_T} ; \quad I_L = \frac{V_L}{R_L}$

Calculate $A_I$

$A_I = \frac{I_L}{I_{in}}$

Calculate $R_{in}$

$R_{in} = \frac{V_{in}}{I_{in}}$
To design a stage which ensures, in the passband, the desired voltage amplification.

\[ A_v = \frac{V_L}{V_{in}} \]

If the load can be selected a possible solution is the:

**common emitter stage**

**Synthesis steps**

1. Synthesize the bias network \((R_1, R_2, R_C, R_E)\).
2. Select the \(R_L\) value which ensures the voltage gain desired.
3. Choose the appropriate values for \(C_1, C_2\) and \(C_3\) \((C_3 >> C_1\ and \ C_2)\) which ensure the lower cutoff frequency given in the project specifications.
Synthesis steps: 1

Synthesis of bias network for the CEC (and CBC)

4 resistors \rightarrow 4 relations

1) \( V_{CC} = R_c I_c + V_{CEQ} + R_E \cdot (I_{CQ} + I_{BQ}) \)

2) \( V_E = \frac{V_{CC}}{10 \div 20} \)

3) \( I_2 \gg I_{BQ} = \frac{I_{CQ}}{h_{FE}} \) \( \Rightarrow I_2 \geq 10 \cdot I_{BQ} = 10 \cdot \frac{I_{CQ}}{h_{FE}} \)

\( R_2 \leq \frac{R_{base}}{10} = \frac{1}{10} \left( \frac{V_{BEQ}}{I_{BQ}} + (1 + h_{FE}) \cdot R_E \right) \) \( \Rightarrow R_2 \leq \frac{1}{10} \cdot h_{FE} \cdot R_E \)

4) \( \frac{V_{CC} \cdot R_2}{R_1 + R_2} = R_1 // R_2 \cdot I_{BQ} + (V_{BEQ} + V_E) \approx (V_{BEQ} + V_E) \)

\( R_1 \approx \frac{V_{CC} - (V_{BEQ} + V_E)}{V_{BEQ} + V_E} \cdot R_2 \)
Synthesis steps: 1

Synthesis steps of bias network:

1) Choose the supply voltage $V_{cc}$ and the transistor working point: $I_c, V_{ce}$.

2) From the datasheet $V_{BEon}$ and $h_{FE}$ values can be obtained. 

\[
V_{BEon} = 0.66 \text{ V} \\
h_{FE} = 210
\]

3) $R_E$ is obtained by:

\[
R_E = \frac{V_E}{I_{CQ}} = \frac{V_{cc}}{20 \cdot I_{CQ}} = \frac{1V}{10mA} = 100 \Omega
\]

4) $R_C$ is obtained by:

\[
R_C = \frac{V_{cc} - V_{CEQ} - V_E}{I_{CQ}} = \frac{9V}{10mA} = 900 \Omega 
\Rightarrow R_C = 820 \Omega
\]

4) $R_2$ is obtained by:

\[
R_2 \leq \frac{1}{10} \cdot h_{FE} \cdot R_E = \frac{210 \cdot 100 \Omega}{10} = 2.1k \Omega \Rightarrow R_2 = 1.8k \Omega
\]

Or:

\[
R_2 = \frac{V_{BE} + V_E}{I_2} \leq \frac{V_{BE} + V_E}{10I_c} h_{FE}
\]

5) $R_1$ is obtained by:

\[
R_1 = \frac{V_{cc} - (V_{BEQ} + V_E)}{V_{BEQ} + V_E} \cdot R_2 = \frac{18.44}{1.66} \cdot 1.8k \Omega \approx 20k \Omega \Rightarrow R_1 = 22k \Omega
\]
**Synthesis steps: 2**

$R_L$ is obtained by circuit analysis.

\[
A_v = -\frac{h_{fe} \cdot (R_C // R_L)}{h_{ie}} \quad \Rightarrow \quad \frac{1}{R_L} = \frac{h_{fe}}{h_{ie} |A_v|} - \frac{1}{R_C}
\]
To design a stage to ensure, in the passband, a voltage amplification

\[ A_v = \frac{V_L}{V_{in}} \]

If the load is fixed a possible solution is the:

**common emitter stage with emitter degeneration**

The emitter resistor is replaced with \( R_E // \text{Series} \ (C_3 - R_3) \) to obtain different impedance values in DC and AC.

**Synthesis steps**

1. Synthesize the bias network \((R_1, R_2, R_C, R_E)\). ⇒ **Same approach of the CEC.**
2. Select the R3 value.
3. Choose the appropriate values for C1, C2 and C3 \((C_3 >> C_1 \text{ and } C_2)\) which ensure the lower cutoff frequency given in the project specifications.
Synthesis steps: 2

\[
A_v = -\frac{h_{fe} \cdot (R_C \parallel R_L)}{h_{ie} + (1 + h_{fe}) R_E \parallel R_3} \approx -\frac{R_C \parallel R_L}{R_E \parallel R_3} \Rightarrow \frac{|A_v|}{R_C \parallel R_L} \approx \frac{1}{R_E \parallel R_3} = \frac{R_E + R_3}{R_E \cdot R_3}
\]

\[
\frac{1}{R_3} \approx \frac{|A_v|}{R_C \parallel R_L} - \frac{1}{R_E}
\]

\[
\frac{1}{R_3} \approx \frac{10}{758 \Omega} - \frac{1}{100 \Omega} = 0.0132 - 0.01 = 0.0032 \Omega^{-1} \quad \Rightarrow \quad R_3 \approx 330 \Omega
\]